File 348:EUROPEAN PATENTS 1978-2003/Nov W04
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File 349:PCT FULLTEXT 1979-2002/UB=20031127,UT=20031120
(c) 2003 WIPO/Univentio

Set	Items	Description
S1	44862	(ERROR? ? OR PARITY)(3N)(CHECK??? OR EXAM? OR TEST??? OR DETECT? OR ANALYZ? OR ANALYS?)
S2	101604	(SECOND? OR 2ND OR TWO OR DUAL? OR SEPARAT? OR DIFFERENT OR ANOTHER OR OTHER)(5W)(MEMORY OR MEMORIES OR RAM OR STORE OR STORES OR STORAGE)
S3	77028	MULTIPLEX?
S4	113	S1(S)S2(S)S3
S5	111	S1(50N)S2(50N)S3
S6	176	S4:S5
S7	1690	S2(15N)S3
S8	457	S1(S)S7 OR S1(50N)S7

8/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01324137
Apparatus and method for digital data transmission
Vorrichtung und Verfahren zur digitalen Datenubertragung
Dispositif et procede de transmission de donnees numeriques
PATENT ASSIGNEE:
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INVENTOR:
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Azenkot, Yehuda, 1128 Littleoak Circle, San Jose, California 95129, (US)
LEGAL REPRESENTATIVE:
Brax, Matti Juhani (85201), Berggren Oy Ab, P.O. Box 16, 00101 Helsinki, (FI)
PATENT (CC, No, Kind, Date): EP 1130918 A2 010905 (Basic)
EP 1130918 A3 020116
APPLICATION (CC, No, Date): EP 2001104540 960725;
PRIORITY (CC, No, Date): US 519630 950825; US 588650 960119; US 684243 960719
DESIGNATED STATES: BE; DE; FR; GB; IE; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 858695 (EP 96927270)
INTERNATIONAL PATENT CLASS: H04N-007/173; H04L-012/28; H04J-011/00; H04J-013/02; H04J-003/06; H04B-001/707; H04L-005/02
ABSTRACT WORD COUNT: 143
NOTE:
Figure number on first page: 49

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200136	11690
SPEC A	(English)	200136	67576
Total word count - document A			79266
Total word count - document B			0
Total word count - documents A + B			79266

...SPECIFICATION are used to encode the digital characters being transmitted. Because of the large number of data points, the differences in phase and amplitude between the **different** points are not large. Therefore, the impairments described above can cause errors by causing misinterpretation by demodulators of what characters were actually sent. There is...
...have been transmitted thereby increasing the error rate. Increased error rate requires more bandwidth to be consumed in retransmitting data and wastes processing power in **detecting** and correcting **errors** and retransmitting data with errors that are beyond the correction range of the ECC bits transmitted with the data.
Also, because in TDMA schemes the...CDMA scheme is to "whiten" the noise sources such that no matter how complex the noise signals, the noise can be effectively managed using conventional **error detection** and correction bits. In other words, the digital data providing the interactive or bidirectional data communication is sent using a CDMA scheme, but for purposes...a symbol will generally not cause errors in the interpretation of symbol 66 by the CU receiver. Each symbol encoded in the code domain includes **error detection** and correction bits (ECC bits) such that any errors that occur can usually be detected and corrected when the symbols are re-constituted by the...the RU performs chip clock synchronization and carrier recovery in the manner described below in the discussion of Figure 19. Carrier recovery is done by **examining** slicer **error** on a known BPSK pilot carrier or pilot channel signal transmitted during a predetermined timeslot using a predetermined code (CU local oscillator signal samples in...invention, and, therefore, the encoders 402 and 526 in Figures 19 and 28A, respectively, could be

eliminated or replaced with simple encoders using any known **error detection** or correction encoding scheme and a mapper to map the resulting encoded symbols into points in a constellation.

In the preferred embodiment, the encoders 402...forward error correction is not used, and the encoder 402 is an ARQ encoder which simply adds enough ECC bits to allow the receiver to **detect** an **error** and request a retransmission. The retransmission request is made on one of the command and control channels. In some block code embodiments, the forward error...

...a trellis code.

The preferred form of the encoder 402 is the 16 state trellis encoder shown in Figure 42. This encoder is characterized by **parity check** polynomials given in octal form as follows: h3=04, h2=10, h1=06, h0=23, d(circumflex)2(underscore)free=5.0, Nfree=1.68...

...memory 404, receives the stream of tribits for each symbol and calculates a 4th redundancy bit for each tribit. This 4th bit provides redundancy for **error detection** and correction and for use by a Viterbi Decoder 468 in the receiver in ascertaining with greater accuracy the data that was actually sent despite...point before the baseband signal enters the slicer so as to minimize interpretation errors caused by amplitude errors. Likewise, a rotational amplifier in the slicer **detector** corrects for phase **errors** caused by the differing propagation delays and channel impairments prior to the baseband signal entering the slicer to minimize this source of errors. For a...a Viterbi Decoder 468 which performs the prior art Viterbi algorithm. The Viterbi Decoder uses the 4th bit in each chip of each symbol to **detect** and correct **errors** . This is done by performing the Viterbi algorithm to derive the most probable tribit path defined by the points actually sent from the path in ...language in block 632 "Look for one pulse in each gap (one SF, Pulse Position Becomes No 1-7)" The steps following block 632 just **check** for **errors** in this process. Specifically, test 634 is performed after each frame to increment a pulse counter and determine if the pulse count has reached 4...errors between the actual received data and the 3-j point are output on bus 798 to the control loop 781. The control loop 781 **examines** these **error** values, and adjusts the 1/a and e-j(o slash)) amplitude and phase error correction factors in an appropriate direction to tend to minimize...

8/3,K/4 (Item 4 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

01272330

COMMUNICATION SYSTEM, FIELD STRENGTH COMPENSATION METHOD IN COMMUNICATION SYSTEM, AND BASE STATION AND TERMINAL STATION FOR RADIO COMMUNICATION SYSTEM

KOMMUNIKATIONSSYSTEM, VERFAHREN ZUR FELDSTARKENKOMPENSATION IN EINEM KOMMUNIKATIONSSYSTEM UND BASISSTATION UND ENDGERAT FUR EIN FUNKKOMMUNIKATIONSSYSTEM

SYSTEME DE COMMUNICATIONS, PROCEDE DE COMPENSATION D'INTENSITE DE CHAMP DANS UN SYSTEME DE COMMUNICATIONS, ET STATION DE BASE ET STATION TERMINALE POUR SYSTEME DE COMMUNICATIONS RADIO

PATENT ASSIGNEE:
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LEGAL REPRESENTATIVE:
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PATENT (CC, No, Kind, Date): EP 1207638 A1 020522 (Basic)
WO 200115342 010301
APPLICATION (CC, No, Date): EP 99938574 990823; WO 99JP4514 990823

DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: H04B-007/26
ABSTRACT WORD COUNT: 123
NOTE:
Figure number on first page: 2

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200221	2666
SPEC A	(English)	200221	9459
Total word count - document A			12125
Total word count - document B			0
Total word count - documents A + B			12125

...SPECIFICATION for correcting the received signal strength indicator, detected by the received signal strength indicator detecting section, according to the correction quantity read out by the **second memory** control section.
With this configuration, in this case, after the information on the number of **multiplexes** of a transmission multiplexed signal from the base station is broadcasted to the terminal station, the terminal station obtains a correction quantity on a received...

...corresponding to the information on the number of multiplexes to correct the received signal strength indicator according to the correction quantity for compensating for an **error** in **detection** of the received signal strength indicator. Accordingly, the detection accuracy on the received signal strength indicator is improvable in the terminal station in addition to...

8/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01094561
DEVICE AND METHOD FOR DATA OUTPUT AND DEVICE AND METHOD FOR DATA INPUT/OUTPUT
VORRICHTNG UND VERFAHREN ZUR DATENAUSGABE UND VORRICHTUNG UND VERFRAHREN ZURDATENEINGABE/AUSGABE
DISPOSITIFS ET PROCEDES DE SORTIE DE DONNEES, ET D'ENTREE/SORTIE DE DONNEES
PATENT ASSIGNEE:
Sony Corporation, (214028), 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001, (JP), (Applicant designated States: all)
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TANAKA, Hisao Sony Corporation, 7-35, Kitashinagawa 6-chome Shinagawa-ku, Tokyo 141-0001, (JP)
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PATENT (CC, No, Kind, Date): EP 992992 A1 000412 (Basic)
WO 9950849 991007
APPLICATION (CC, No, Date): EP 99910695 990325; WO 99JP1508 990325
PRIORITY (CC, No, Date): JP 9881270 980327
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G11B-020/10; G06F-003/06
ABSTRACT WORD COUNT: 121
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200015	1522
SPEC A	(English)	200015	5613
Total word count - document A			7135
Total word count - document B			0
Total word count - documents A + B			7135

...SPECIFICATION so that they may correspond to each of the plurality of HDDs 13b1, 13b2, ---, 13bn and then, an arithmetic of error correction coding data (for **example** , **parity** data) in relation to respective bit data is performed so that the parity data may be written to the HDD 13bn. Further, when performing process...

...the HDDs 13b1, 13b2, ---, 13bn, the parity data recorded on the HDD 13bn are read and after error correction is performed thereon, the data are **multiplexed** and outputted.
As data transfer rate of the data bus 20 is **different** from that from buffer **memory** 13e to the buffer memories 13c1, 13c2, ---, 13cn, the buffer memory 13e is memory used for reducing the difference of their data transfer rate.
Bus...

8/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00996862
Start code detecting apparatus for video data stream
Vorrichtung zur Startkodedetektierung fur Videodatenstrom
Appareil de detection de code de depart pour un flux de donnees video
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (Applicant designated States: all)
INVENTOR:
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Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-under-edge, Gloucester GL12 7ND, (GB)
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PATENT (CC, No, Kind, Date): EP 901287 A2 990310 (Basic)
EP 901287 A3 990922
APPLICATION (CC, No, Date): EP 98202166 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-013/00; G06F-009/38
ABSTRACT WORD COUNT: 112
NOTE:
Figure number on first page: 61

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9910	191
SPEC A	(English)	9910	126718
Total word count - document A			126909
Total word count - document B			0
Total word count - documents A + B			126909

...SPECIFICATION stages in the pipeline are afforded enhanced flexibility in configuration and processing.

Each of the processing stages in the pipeline may include both primary and **secondary storage**, and the stages in the pipeline are reconfigurable in response to recognition of selected tokens. The tokens in the pipeline are dynamically adaptive and may...7:0).

Thus, the first time a given MID(underscore)DATA is loaded into LEOUT, the associated OUTEXTN will be forced high, whereas, on the **second** occasion, OUTEXTN will be the same as the signal QEIN. Now consider the situation during the very last word of a token in which QEIN...systems to indicate a channel or media error. For example, this start code may be inserted into the data by an ECC circuit if it **detects** an **error** that it was unable to correct.

A.11.4.4 Sequence of event generation

In the present invention, certain coded data patterns (probably indicating an...

8/3,K/8 (Item 8 from file: 348)

00964844

Reconfigurable image processing pipeline
Rekonfigurierbares Pipeline-Bildverarbeitungssystem
Systeme de traitement d'image pipeline reconfigurable

PATENT ASSIGNEE:
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Pulver, Mark, c/o Canon Inf.Syst.Res.A.PTY LTD, 1 Thomas Holt Drive, North Ryde, New South Wales 2113, (AU)
Webb, Michael J., c/o Canon Inf.Syst.Res.A.PTY LTD, 1 Thomas Holt Drive, North Ryde, New South Wales 2113, (AU)
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PATENT (CC, No, Kind, Date): EP 875854 A2 981104 (Basic)
EP 875854 A3 030813
APPLICATION (CC, No, Date): EP 98303362 980429;
PRIORITY (CC, No, Date): AU 97PO6479 970430; AU 97PO6480 970430; AU 97PO6481 970430; AU 97PO6482 970430; AU 97PO6483 970430; AU 97PO6484 970430; AU 97PO6485 970430; AU 97PO6486 970430; AU 97PO6487 970430; AU 97PO6488 970430; AU 97PO6489 970430; AU 97PO6490 970430; AU 97PO6491 970430; AU 97PO6492 970430
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06T-001/20
ABSTRACT WORD COUNT: 174
NOTE:
Figure number on first page: 129
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9845	10768
SPEC A	(English)	9845	65006
Total word count - document A			75774
Total word count - document B			0
Total word count - documents A + B			75774

...SPECIFICATION accessed from the cache by the processing unit at a time. In image processor systems where the processing unit requires several items of data from **separate** tables in **memory** to perform an operation, it would be advantageous if all the data is supplied to the processing unit in one data packet.

A further problem...Firstly, in printing pages it is necessary that there not be even small or transient artefacts. This is because whilst in video signal creation for **example** . such small **errors** if present may not be apparent to the human eye (and hence be unobservable). in printing any small artefact appears permanently on the printed page...signal "reg" output from the read/write controller 352.

The exception generators 356-359 generate an output error signal, eg. 347-349, 362 when an **error** is **detected** on their inputs. The formula for calculating each output error is as aforementioned.

The register components 360 can be defined to be of a number...for each module that can operate in a background mode in addition to any preset, error and interrupt lines, one for each module, for resetting, **detecting errors** and interrupts.

3.15 Co-processor Data Types and Data Manipulation

Returning now to Fig. 2, in order to substantially simplify the operation of the...

8/3,K/9 (Item 9 from file: 348)

00938459

TRANSMITTER, RECEIVER, TRANSMISSION SYSTEM, SENDING METHOD, RECEIVING METHOD, AND TRANSMITTING METHOD

SENDER, EMPFANGER, UBERTRAGUNGSSYSTEM, SENDEVERFAHREN , EMPFANGSVERFAHREN UND UBERTRAGUNGSVERFAHREN

EMETTEUR, RECEPTEUR, SYSTEME DE TRANSMISSION, PROCEDE D'EMISSION, PROCEDE DE RECEPTION ET PROCEDE DE TRANSMISSION

PATENT ASSIGNEE:
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NISHIOKA Minoru, 2-1-20-510, Uozaki-nishimachi Higashinada-ku, Kobe-shi Hyogo 658, (JP)
BANNAI, Tatsushi, 389-12, Kitanoda Sakai-shi, Osaka 588, (JP)
NISHINO, Masakazu, 1-4-26, Kamiichi Kashiwara-shi, Osaka 582, (JP)

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PATENT (CC, No, Kind, Date): EP 939513 A1 990901 (Basic)
WO 9810557 980312
APPLICATION (CC, No, Date): EP 97939204 970905; WO 97JP3142 970905
PRIORITY (CC, No, Date): JP 96234858 960905; JP 9745603 970228; JP 97189400 970715
DESIGNATED STATES: DE; GB; NL
RELATED DIVISIONAL NUMBER(S) - PN (AN):
(EP 2002014215)
INTERNATIONAL PATENT CLASS: H04L-007/08; H04L-001/00; H03M-007/40; H04J-003/00; H04N-007/00
ABSTRACT WORD COUNT: 158

NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9935	16117
SPEC A	(English)	9935	68029
Total word count - document A			84146
Total word count - document B			0
Total word count - documents A + B			84146

...SPECIFICATION designate variable-length coding means in the same way; by these means, compressing means 4a to 4c are formed respectively. The numeral 16 designates a **multiplexing** means which temporarily **stores** each of the output signals of the variable- ...error correction code to each block of video signal, a constant information unit, from the output signal of the multiplexing means 16; the receiving apparatus **detects** or corrects code **errors** on the basis of the error correction code. The present embodiment uses the Reed-Solomon code as an error correction code.
The lower half portion...

8/3,K/10 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00907399
Dynamic mapping of broadcast resources
Dynamische Zuteilung von Rundfunkubertragungen
Allocation dynamique de ressources de telediffusion
PATENT ASSIGNEE:
Hughes Electronics Corporation, (2464050), 200 N. Sepulveda Boulevard, El Segundo, California 90245-0956, (US), (Applicant designated States: all)
INVENTOR:
Arsenault, Robert G., 2815 May Avenue, Redondo Beach, CA 90278, (US)
Leminh, Tam T., 4709 Montefino Drive, Cypress, CA 90630, (US)
James, Thomas H., 1010 Fiske Street, Pacific Palisades, CA 90272, (US)
LEGAL REPRESENTATIVE:
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PATENT (CC, No, Kind, Date): EP 828390 A2 980311 (Basic)
EP 828390 A3 990908
APPLICATION (CC, No, Date): EP 97115360 970904;
PRIORITY (CC, No, Date): US 708524 960905
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: H04N-007/16
ABSTRACT WORD COUNT: 137
NOTE:
Figure number on first page: 4

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9811	1908
SPEC A	(English)	9811	14867
Total word count - document A			16775
Total word count - document B			0
Total word count - documents A + B			16775

...SPECIFICATION with the present invention. Although the complete local map may preferably be transmitted occasionally (to permit activation of new equipment and provide a periodic integrity **check** to correct any **errors**), such full map transmissions are reduced.
To further minimize transmission requirements for map changes, a plurality of complete maps may be transmitted and stored locally. For

example, a first complete map can be transmitted and stored, followed by a **second** complete map stored in **other memory** . The receiving apparatus includes a map selector (e.g. selection vector, **multiplexor** , etc.) which selects the stored map that is to be active at a given time. To accomplish a change in local mapping, it is then...

8/3,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00887645
Management of overflowing data in a computer system
Datenuberlaufverwaltung in einem Rechnersystem
Gestion de debordement de donnees dans un systeme d'ordinateur
PATENT ASSIGNEE:
Compaq Computer Corporation, (687792), 20555 S.H. 249, Houston Texas 77070, (US), (applicant designated states: AT;BE;CH;DE;DK;ES;FI;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)
INVENTOR:
Pettey, Christopher J., 9327 Rodgers Road, Houston, Texas 77070, (US)
Maclaren, John M., 15318 Redbud Leaf Lane, Cypress, Texas 77429, (US)
LEGAL REPRESENTATIVE:
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PATENT (CC, No, Kind, Date): EP 811934 A2 971210 (Basic)
EP 811934 A3 990210
APPLICATION (CC, No, Date): EP 97303804 970604;
PRIORITY (CC, No, Date): US 658533 960605
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-013/40;
ABSTRACT WORD COUNT: 93

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9712W1	593
SPEC A	(English)	9712W1	59351
Total word count - document A			59944
Total word count - document B			0
Total word count - documents A + B			59944

...SPECIFICATION the first data storage buffer.
Embodiments of the invention may include one or more of the following features. The buffer management element may assign the **second storage** buffer only if the **second storage** buffer does not contain data associated with another data transaction stored in the bridge. The buffer storage element may assign a third storage buffer, if...address cycle or a posted memory write request, the slave state machine loads the dword counter (asserts load(underscore)write(underscore)counter) and, if no **parity error** has occurred, **analyzes** the delayed request transaction. If the transaction is a MRL or a MRM transaction and the QPIF lock logic is not in the unlocked-but...
...the PMW1 state 2724.
If the transaction is not a posted memory write request, the slave state machine loads the dword counter and, if no **parity error** has occurred, **analyzes** the delayed request transaction. If the transaction is a MRL or a MRM transaction and the QPIF lock logic is not in the unlocked-but...to-upstream data transfer format. The following is a description of the signals.
EDC(7:0): The signals are the eight syndrome bits used to **detect** and correct **errors** encountered in transmitting data over the cable 28.
CAD(31:0): The signals are the 32 address or data bits.
CFRAME(underscore): The signal is...discharges from the signal pins when the connector is disconnected. A pair of thumb screws attached to the cable connector will secure the mated connectors.

ERROR DETECTION AND CORRECTION

An **error detection** and correction (EDC) method is implemented on each bridge chip to protect communication over the cable 28. Since the data is time-multiplexed into three...

...28 (which pass such information as the clock signals CABLE(underscore)CLK1 and CABLE(underscore)CLK2, reset signals, and the power good/PLL-lock signal), **error detection** and correction is not implemented.

The following are the underlying assumptions for the EDC algorithm. Most errors are single bit errors. The probability of having...

...provided to the input of a check bit generator 350, which produces check bits CHKBIT(7:0). The check bits are generated according to the **parity - check** matrix shown in Figure 18, in which the first row corresponds to CHKBIT(0), the second row corresponds to CHKBIT(1), and so forth. The...

...generated by an exclusive-OR of all the data bits FIFOOUT(X) (X is equal to 0-59), which have a "1" value in the **parity - check** matrix. Thus, the check bit CHKBIT(0) is an exclusive-OR of data bits FIFOOUT(7), FIFOOUT(8), FIFOOUT(9), FIFOOUT(12), FIFOOUT(13), FIFOUT...

...27, 35, 37, 38, 40, 43, 46, 47, 48, 50, and 53. Check bits CHKBIT(2:7) are generated in similar fashion according to the **parity - check** matrix of Figure 18. The **parity check** matrix is based upon the 20 sub-channels or wires per time-multiplexed phase and a probability that multiple errors in the accumulated data are...

...same data position in each time-multiplexed phase.

In the master cable interface 192 or 194, the check bits CHKBIT(7:0) are provided as **error detection** and Correction bits EDC(7:0) along with other cable data to allow error correction logic in the slave cable interface 196 or 198 to **detect** and correct data **errors** .

The **check** bits CHKBIT(7:0) are provided to a fix bit generator 352, which generates fix bits FIXBIT(59:0) according to the syndrome table shown...one of each the lower 52 bits of the FIFO data FIFOOUT(51:0). The upper 8 FIFO bits FIFOOUT(59:52), allocated to the **error detection** and correction bits EDC(7:0), are used to generate the check bits and the syndrome bits, but are not subject to error correction. The...

...by a configuration signal CFG2C(underscore)ENABLE(underscore)ECC. The output of the multiplexer 360 produces signals MUXMSGI(51:0). If the system software enables **error detection** and correction by setting the signal CFG2C(underscore)ENABLE(underscore)ECC high, then the multiplexer 360 selects the corrected data CORRMSG(51:0) for output. Otherwise, if **error detection** and correction is disabled, the data bits FIFOOUT(51:0) are used.

The non-correctable and correctable error indicators NCERR and CRERR are provided to...

...358 produce signals C(underscore)NLERR and C(underscore)CRERR, respectively. The signals C(underscore)NLERR and C(underscore)CRERR can be asserted only if **error detection** and correction is enabled. When an **error** is **detected** , the fix bits are latched and used for diagnostic purposes.

If a correctable error is indicated (the signal C(underscore)CRERR is high), then an...

...to be negated so that the upstream bridge chip 26 does not send cycles downstream.

To prevent spurious interrupts during and just after power-up, **error detection** and correction on both the upstream and downstream bridge chips is disabled during power-up until the upstream PLL 186 and downstream PLL 182 have...

8/3,K/13 (Item 13 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00854676
DATA ERROR DETECTION AND CORRECTION FOR A SHARED SRAM
DATENFEHLER-DETEKTION UND -KORREKTUR FUR GEMEINSAMEN SPEICHER
DETECTION ET CORRECTION D'ERREURS POUR UNE MEMOIRE RAM STATIQUE PARTAGEE
PATENT ASSIGNEE:
Honeywell Inc., (246054), Honeywell Plaza MN12-8251 P.O. Box 524, Minneapolis Minnesota 55440-0524, (US), (Proprietor designated states: all)
INVENTOR:
LORDI, Angela, L., 2043 Fort Bevon Road, Harleysville, PA 19438, (US)
LEGAL REPRESENTATIVE:
Fox-Male, Nicholas Vincent Humbert (57744), Eric Potter Clarkson Park View House 58 The Ropewalk, Nottingham NG1 5DD, (GB)
PATENT (CC, No, Kind, Date): EP 862761 A2 980909 (Basic)
EP 862761 B1 991222
WO 9714109 970417
APPLICATION (CC, No, Date): EP 96937661 961007; WO 96US16037 961007
PRIORITY (CC, No, Date): US 541989 951010
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-011/16
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	199951	1010
CLAIMS B	(German)	199951	1017
CLAIMS B	(French)	199951	1189
SPEC B	(English)	199951	2539
Total word count - document A			0
Total word count - document B			5755
Total word count - documents A + B			5755

...SPECIFICATION any extra time.

SUMMARY OF INVENTION
Thus, there is provided by the present invention, which is defined in the appended independent claims, a scheme for **error detection** and correction which does not require any extra time to perform the correction. An apparatus for correcting errors in information read from a memory unit...

...primary information and the backup information are coupled to the two sets of input ports of the multiplexer. Select logic is operatively connected to the **multiplexer** , and further is operatively connected to the first memory and to the **second memory** . The first and **second memory** each equipped with **parity detection** logics indicate via a respective first and second error signal if an **error** is **detected** on the information just read from the first and second memory, respectively. The select logic determines whether the data in the first and second memory...

...CLAIMS from the lower memory of the first and second memories (10, 11) and the backup information read from the upper memory of the first and **second memories** (10, 11) are coupled to the first and second input ports of the **multiplexer** (40); and
e) select logic (50), operatively connected to said **multiplexer** (40), and further operatively connected to said first memory (10) and to said **second memory** (11), the first (10) and second memory (11) indicating via the respective first (P1) and second error signal (P2) if an **error** is **detected** on the information just read from the first (10) and second memory (11), respectively, the select logic (50) determines whether the data in the first...

8/3,K/15 (Item 15 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00804145
Circuit and method for biasing bit lines
Schaltung und Verfahren um Bitleitungen vorzuspannen
Circuit et methode pour la polarisation de lignes de bit
PATENT ASSIGNEE:
STMicroelectronics, Inc., (723066), 1310 Electronics Drive, Carrollton Texas 75006-5039, (US), (Proprietor designated states: all)
INVENTOR:
McClure, David C., 3701 Elizabeth Drive, Carrollton, Texas 75007, (US)
LEGAL REPRESENTATIVE:
Palmer, Roger et al (34631), PAGE, WHITE & FARRER 54 Doughty Street, London WC1N 2LS, (GB)
PATENT (CC, No, Kind, Date): EP 747824 A1 961211 (Basic)
EP 747824 B1 030205
APPLICATION (CC, No, Date): EP 96303448 960515;
PRIORITY (CC, No, Date): US 484491 950607
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G06F-011/20
ABSTRACT WORD COUNT: 65
NOTE:
Figure number on first page: 4

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	1068
CLAIMS B	(English)	200306	1343
CLAIMS B	(German)	200306	1392
CLAIMS B	(French)	200306	1524
SPEC A	(English)	EPAB96	2251
SPEC B	(English)	200306	2761
Total word count - document A			3320
Total word count - document B			7020
Total word count - documents A + B			10340

...SPECIFICATION substitute redundant column may simultaneously try to load data onto the data bus during a read operation. Such simultaneous data loading may cause a read **error** . An **example** of the first type of memory device is disclosed in U.S. Patent No. 5,355,340, which issued to Coker et al. on 11 October 1994 and is incorporated by reference herein.

In the **second** type of existing **memory** device, because the data from the matrix and redundant columns is **multiplexed** onto the data bus, the defective column need not be disconnected to prevent data errors. The defective column, however, is often disconnected from the read...

...SPECIFICATION substitute redundant column may simultaneously try to load data onto the data bus during a read operation. Such simultaneous data loading may cause a read **error** . An **example** of the first type of memory device is disclosed in U.S. Patent No. 5,355,340, which issued to Coker et al. on 11 October 1994.
In the **second** type of existing **memory** device, because the data from the matrix and redundant columns is **multiplexed** onto the data bus, the defective column need not be disconnected to prevent data errors. The defective column, however, is often disconnected from the read...

8/3,K/16 (Item 16 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00779023
Continuous data server apparatus and data transfer scheme enabling multiple simultaneous data accesses
Server fur kontinuierliche Daten und Datentransferschema fur mehrfache gleichzeitige Datenzugriffe

Serveur donnees continues et methode de transfert de donnees permettant de . multiples acces simultanes de donnees

PATENT ASSIGNEE:
KABUSHIKI KAISHA TOSHIBA, (213130), 72, Horikawa-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken 210, (JP), (applicant designated states: DE;FR;GB;SE)
INVENTOR:
Kanai, Tatsunori, 1351-B203, Yabe-cho, Totsuka-ku, Yokohama-shi, Kanagawa-ken, (JP)
Asano, Shigehiro, 3-1-1-105, Nobi, Yokosuka-shi, Kanagawa-ken, (JP)
Aikawa, Takeshi, 2-44-2, Kamiishihara, Choufu-shi, Tokyo, (JP)
Amano, Shinya, 2-311, 2-22, Serigaya, Kounan-ku, Yokohama-shi, Kanagawa-ken, (JP)
LEGAL REPRESENTATIVE:
Zangs, Rainer E., Dipl.-Ing. et al (72561), Hoffmann, Eitle & Partner Arabellastrasse 4/VIII, 81925 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 727750 A2 960821 (Basic)
EP 727750 A3 970723
APPLICATION (CC, No, Date): EP 96102361 960216;
PRIORITY (CC, No, Date): JP 9529749 950217; JP 95236999 950914; JP 95253293 950929; JP 95315578 951204
DESIGNATED STATES: DE; FR; GB; SE
INTERNATIONAL PATENT CLASS: G06F-017/30; G06F-003/06; G06F-011/10;
ABSTRACT WORD COUNT: 215

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	3141
SPEC A	(English)	EPAB96	28993
Total word count - document A			32134
Total word count - document B			0
Total word count - documents A + B			32134

...SPECIFICATION is a case in which the data are to be read out from another buffer memory 108 not corresponding to it, and no malfunction or **error** is **detected** in the disk device 102 corresponding to itself as well as in the disk device 102 corresponding to that **another** buffer **memory** 108, in which case the output of the **multiplexer** 132 is switched to the A input.

A case (3) of Fig. 34 is a case in which the data are to be read out from another buffer memory 108 not corresponding to it, and no malfunction or **error** is **detected** in the disk device 102 corresponding to itself but a malfunction or **error** is **detected** in the disk device 102 corresponding to that **another** buffer **memory** 108, in which case the output of the **multiplexer** 132 is switched to the B input.

A case (4) of Fig. 34 is a case in which the data should be read out from the corresponding buffer memory 108, and no malfunction or **error** is **detected** in the corresponding disk device 102, in which case the output of the multiplexer 132 is switched to the B input.

A case (5) of...

...is a case in which the data are to be read out from another buffer memory 108 not corresponding to it, and a malfunction or **error** is **detected** in the disk device 102 corresponding to itself but no malfunction or **error** is **detected** in the disk device 102 corresponding to that **another** buffer **memory** 108, in which case the output of the **multiplexer** 132 is switched to the A input.

As shown in Fig. 30, the first stage calculation unit 103 in the series connection has an input...

8/3,K/17 (Item 17 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00741338

Connectionless communications system, test method, and intra-station control system

Verbindungsloses Kommunikationssystem, Testmethode und Intra-Station-Steuerungssystem

Systeme de communication sans connection, methode de test et systeme de gestion intra-station

PATENT ASSIGNEE:
FUJITSU LIMITED, (211460), 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa 211, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Kobayasi, Yasusi, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Watanabe, Yoshihiro, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Nishida, Hiroshi, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Izawa, Naoyuki, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Murayama, Masami, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Abe, Jin, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Uchida, Yoshihiro, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Yamanaka, Hiromi, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Aso, Yasuhiro, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Tsuruta, Yoshihisa, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Kato, Yoshiharu, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Kakuma, Satoshi, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Uriu, Shiro, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Samejima, Noriko, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Ishioka, Eiji, Fujitsù Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Sekine, Shigeru, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Karakawa, Yoshiyuki, Fujitsu Kyushu Communication, Systems Ltd., Yasudaseimeihakata Blg., 1-4-4,, Hakataekimae, Hakata-ku, Fukuoka, 812, (JP)
Kagawa, Atsushi, c/o Fujitsu Communication, Systems Ltd., 3-9-18, Shinyokohama, Kouhoku-ku, Yokohama-shi, Kanagawa, 222, (JP)
Nakayama, Mikio, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
Kawataka, Miyuki, Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
LEGAL REPRESENTATIVE:
Ritter und Edler von Fischern, Bernhard, Dipl.-Ing. et al (9672), Hoffmann, Eitle & Partner, Patentanwalte, Arabellastrasse 4, D-81925 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 700229 A2 960306 (Basic)
EP 700229 A3 990203
APPLICATION (CC, No, Date): EP 95113111 950821;
PRIORITY (CC, No, Date): JP 94255120 940822
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H04Q-011/04
ABSTRACT WORD COUNT: 170

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	8491
SPEC A	(English)	EPAB96	164543

Total word count - document A 173034
Total word count - document B 0
Total word count - documents A + B 173034

...SPECIFICATION in the BSGC.
(Figure 717) shows the configuration of the hardware relating to the INF.
(Figure 718) shows the bit configuration between the MM (main **memory**) and BSGC of the data DMA-transferred.
(Figure 719) shows the congestion control of the receiving system.
(Figure 720) shows a model of the number...1 Loopback Function of Cell provided with "0" bit
7.14.2 Loopback Function of Cell provided with specific VCI/VCI
7.15 MSCN Data **Multiplexing** Function
7.16 MSD Data Dropper Function
8. Maintenance Signal Driver (MSD) Interface
8.1. MSD Information
8.1.1. E-MSD Hardware Interface
8...to the SIFCOM of the fault monitor object system as shown in Figure 156.

8.1.3.3. Power Package Missing Fault
This fault is **detected** by monitoring the state of the loop signal line in the SIFCOM of the mate system to the SIFCOM of the fault monitor object system...

...Fuse Disconnection Fault
This fault is described in 14.1.5. in part 2.

8.1.4.2. SIFCOM Fuse Disconnection Fault
This fault is **detected** by monitoring the state of the signal line connected to the SIFCOM fuse in the SIFCOM of the mate system to the SIFCOM of the...signal indicating the existence of cable connection has an interface having a circuit configuration of a transistor logic (TTL) through a non-balanced transmission.
A **parity** refers to an odd parity for 8-bit parallel data excluding an enable signal. **Parity** bits of valid cells only are checked in the input unit of the ATM switch, and parity bits are assigned to valid cells only in...collect the fault information in the ASSWSH-A and to notify a higher order device (CC) of the fault information.
Figure 200 shows the fault **detection** procedure followed when a notification is made by the MSCN. Figure 201 shows the fault detection procedure followed when a status is autonomously notified of...

8/3,K/18 (Item 18 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00545839
Write overlap with overwrite prevention
Schreibuberlappung mit Verhinderung des Uberschreibens
Ecriture a chevauchement avec prevention de superposition d'ecriture
PATENT ASSIGNEE:
SUN MICROSYSTEMS, INC., (1392730), 2550 Garcia Avenue, Mountain View, CA 94043, (US), (Proprietor designated states: all)
INVENTOR:
Chesley, Gilman, 1010 Pelton Avenue, Santa Cruz, California 95060, (US)
LEGAL REPRESENTATIVE:
Wombwell, Francis (46021), Potts, Kerr & Co. 15, Hamilton Square, Birkenhead Merseyside L41 6BR, (GB)
PATENT (CC, No, Kind, Date): EP 547769 A1 930623 (Basic)
EP 547769 B1 991013
APPLICATION (CC, No, Date): EP 92310524 921118;
PRIORITY (CC, No, Date): US 809667 911218
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: G06F-009/38

ABSTRACT WORD COUNT: 143
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9941	780
CLAIMS B	(German)	9941	717
CLAIMS B	(French)	9941	974
SPEC B	(English)	9941	3212
Total word count - document A			0
Total word count - document B			5683
Total word count - documents A + B			5683

...SPECIFICATION through two pipelines in the memory controller 16. Data which is to be read from the memory flows from the memory bus 24, through the **error detection** and correction module 70, through the data out queue 52, to the system bus 12. Data which is to be written to the memory, flows from the system bus 12, to the data-in queue 50, through **multiplexor** 72 to the memory bus 24. By providing **two** distinct data pipelines, the **memory** controller 16 allows for a degree of overlap in memory operations. In particular, a write operation can be overlapped over a preceding read operation. For...

8/3,K/20 (Item 20 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00480869
Integrated data link controller with synchronous link interface and asynchronous host processor interface
Integrierte Datenubertragungsstreckensteuerung mit synchroner Leitungsschnittstelle und asynchroner Host-Prozessor-Schnittstelle
Dispositif integre de commande d'une voie de donnees avec interface synchrone de liaison et interface asynchrone avec le processeur hote
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: BE;CH;DE;ES;FR;GB;IT;LI;NL;SE)
INVENTOR:
Farrell, Joseph Kevin, 4713 Tortoise Shell Drive, Boca Raton, Florida 33487, (US)
Gordon, Jeffrey Scott, 5107 Woodmere Drive, No. 203 Centreville, Virginia 22020, (US)
Jenness, Robert V., 1499 West Royal Palm Road, Boca Raton, Florida 33486, (US)
Kuhl, Daniel C., 16416 Cherry Way, Delray Beach, Florida 33484, (US)
Lee, Timothy Vincent, 1798 S.W. 11th Street, Boca Raton, Florida 33486, (US)
Parker, Tony Edwin, 1745 N.W. 4th Avenue. Unit No. 5, Boca Raton, Florida 33432-1545, (US)
LEGAL REPRESENTATIVE:
Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 447054 A2 910918 (Basic)
EP 447054 A3 951025
EP 447054 B1 990107
APPLICATION (CC, No, Date): EP 91301499 910225;
PRIORITY (CC, No, Date): US 495810 900315
DESIGNATED STATES: BE; CH; DE; ES; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: H04L-029/06;
ABSTRACT WORD COUNT: 233

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count

CLAIMS B	(English)	9901	4873
CLAIMS B	(German)	9901	4464
CLAIMS B	(French)	9901	6004
SPEC B	(English)	9901	66251
Total word count - document A			0
Total word count - document B			81592
Total word count - documents A + B			81592

8/3,K/21 (Item 21 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00424595

Apparatus and method for accessing a cyclic redundancy error check code generated in parallel.

Gerat und Verfahren zur Realisierung eines zyklischen redundanten Parallel-Fehlerprufungskodes.

Appareil et methode pour la realisation d'un code de verification d'erreur cyclique en parallele.

PATENT ASSIGNEE:
NATIONAL SEMICONDUCTOR CORPORATION, (262383), 2990 Semiconductor Drive, Santa Clara, CA. 95051-8090, (US), (applicant designated states: DE;FR;GB;IT)

INVENTOR:
Perloff, Ronald S., 14065 Willow Ranch Road, Poway, CA 92064, (CA)

LEGAL REPRESENTATIVE:
Sparing Rohl Henseler Patentanwalte European Patent Attorneys (100362), Rethelstrasse 123, W-4000 Dusseldorf 1, (DE)

PATENT (CC, No, Kind, Date): EP 431416 A2 910612 (Basic)
EP 431416 A3 920429

APPLICATION (CC, No, Date): EP 90122381 901123;

PRIORITY (CC, No, Date): US 445964 891204

DESIGNATED STATES: DE; FR; GB; IT

INTERNATIONAL PATENT CLASS: H03M-013/00;

ABSTRACT WORD COUNT: 213

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1761
SPEC A	(English)	EPABF1	7843
Total word count - document A			9604
Total word count - document B			0
Total word count - documents A + B			9604

...CLAIMS the second storage elements as the system output signal; and
J) means for iteratively utilizing Element I to transfer out the plurality of groups of **error check** code terms comprising the **error check** code signal.

6. The system of Claim 5, wherein the means for selecting between the received data byte and the **error check** code terms in the last of the **second storage** elements is a **multiplexor** .

7. The system of Claim 5, wherein the

8/3,K/22 (Item 22 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00413007

Pipelined error checking and correction for cache memories

Pipelinefehlerprufung und Korrektur fur Cache-Speicher

Verification et correction d'erreur pipeline pour ante-memoires

PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)

INVENTOR:

Chao, Hu Herbert, 4 Stella Lane, Pleasantville, New York 10570, (US)
Chang, Jung-Herng, 13275 Glasgow Court, Saratoga, California 95070, (US)
LEGAL REPRESENTATIVE:
Rach, Werner, Dr. et al (76871), IBM Deutschland Informationssysteme GmbH, Patentwesen und Urheberrecht, 70548 Stuttgart, (DE)
PATENT (CC, No, Kind, Date): EP 418457 A2 910327 (Basic)
EP 418457 A3 920318
EP 418457 B1 971001
APPLICATION (CC, No, Date): EP 90105210 900320;
PRIORITY (CC, No, Date): US 409362 890919
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-011/10;
ABSTRACT WORD COUNT: 170

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9709W4	447
CLAIMS B	(German)	9709W4	436
CLAIMS B	(French)	9709W4	504
SPEC B	(English)	9709W4	3161
Total word count - document A			0
Total word count - document B			4548
Total word count - documents A + B			4548

...CLAIMS output with the check bits in the cache array (12) at an address corresponding to a content of said fourth register (34).
2. The pipelined **error checking** and correcting cache memory as recited in claim 1 further comprising a first multiplexer (45) responsive to outputs from the cache array and the seventh...

...the same as said third register (33) following a store cycle, in which case the output of said seventh register (42) is selected by said **multiplexer** .
3. A cache memory array as defined in claim 1 providing an effective **two** port **memory** array with the density of a single port array comprising:
an array of single port static random access memory cells (50, 51, 52, 53) connected...

8/3,K/23 (Item 23 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00410147
MEMORY CONTROL UNIT.
STEUEREINHEIT FUR DEN SPEICHER.
UNITE DE COMMANDE DE MEMOIRE.
PATENT ASSIGNEE:
WANG LABORATORIES, INC., (333561), One Industrial Avenue, M/S 014-B7D, Lowell, MA 01851, (US), (applicant designated states: BE;DE;FR;GB;NL)
INVENTOR:
BECKER, Robert, D., 522 E. Groton Road, Shirley, MA 01464, (US)
SCHWARTZ, Martin, J., 16 Rittenhouse Road, Worcester, MA 01602, (US)
CURCUR, Kevin, H., 128 Lowell Road, Pepperell, MA 01463, (US)
ENG, Kenneth, J., 28 Mile Brook Road, West Bridgewater, MA 02379, (US)
LEGAL REPRESENTATIVE:
Behrens, Dieter, Dr.-Ing. et al (1701), Wuesthoff & Wuesthoff Patent- und Rechtsanwalte Schweigerstrasse 2, W-8000 Munchen 90, (DE)
PATENT (CC, No, Kind, Date): EP 425550 A1 910508 (Basic)
EP 425550 A1 920325
WO 9000284 900111
APPLICATION (CC, No, Date): EP 89908327 890622; WO 89US2721 890622
PRIORITY (CC, No, Date): US 213395 880630
DESIGNATED STATES: BE; DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: G06F-013/00;
NOTE:

No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF2	1389
CLAIMS B	(German)	EPBBF2	1064
CLAIMS B	(French)	EPBBF2	1677
SPEC B	(English)	EPBBF2	8478
Total word count - document A			0
Total word count - document B			12608
Total word count - documents A + B			12608

...SPECIFICATION when an address is stored and is reset when the corresponding write operation is accomplished. One of the write addresses is selected by 8 input **multiplexer** 134 which supplies the write address to the memory address **multiplexer** 96. **Other** inputs to the **memory** address **multiplexer** 96 include the refresh address from the refresh address counter 98 and a read address from a four input read address multiplexer 134. Address **parity** logic 136 **detects parity errors** which may occur on the input read and write addresses. The output of memory address multiplexer 96 is latched by a memory address output latch ...

8/3,K/25 (Item 25 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00367283
Data error detection and correction
Datenfehler-Detektion und -Korrektur
Detection et correction d'erreurs dans les donnees
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
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LEGAL REPRESENTATIVE:
Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 352937 A2 900131 (Basic)
EP 352937 A3 911204
EP 352937 B1 960508
APPLICATION (CC, No, Date): EP 89307076 890712;
PRIORITY (CC, No, Date): US 225976 880729
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H03M-013/00; H03M-005/16; H03M-005/20; H03K-019/00;
ABSTRACT WORD COUNT: 129

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	3605
CLAIMS B	(English)	EPAB96	3729
CLAIMS B	(German)	EPAB96	3084
CLAIMS B	(French)	EPAB96	4061
SPEC A	(English)	EPABF1	17168
SPEC B	(English)	EPAB96	16881
Total word count - document A			20774
Total word count - document B			27755
Total word count - documents A + B			48529

...CLAIMS device.
15. A system as claimed in any of claims 9 to 14, wherein the data corrector includes:
a multiplexor unit connected to the single **error detector** and to an incrementor unit and to a decrementor unit and to the second

trinary storage device;
a decrementor unit connected to the **multiplexor** unit and to the **second** trinary **storage** device;
an incrementor unit connected to the **multiplexor** unit and to the **second** trinary **storage** device;
the decrementor unit receiving the data tryte from the second trinary storage device and decrementing each trit of the data tryte one trinary level;
the incrementor unit receiving the data tryte from the **second** trinary **storage** device and incrementing each trit of the data tryte one trinary level;
the **multiplexor** unit receiving: each incremented trit from the incrementor unit, each decremented trit from the decrementor unit, each data tryte from the **second** trinary **storage** device, and each of the output signals from the single **error detector** ;
wherein the **multiplexor** unit under control of the output signals from the single **error detector** selects either the incremented trit, or the decremented trit, or the data trit for each trit position of the tryte for gating the selected trits...

...CLAIMS 15. A system as claimed in any of claims 9 to 14, wherein the data corrector comprises:
a multiplexor unit (570) connected to the single **error detector** and to an incrementor unit and to a decrementor unit and to the second trinary storage device;
a decrementor unit (540) connected to the **multiplexor** unit and to the **second** trinary **storage** device;
an incrementor unit (520) connected to the **multiplexor** unit and to the **second** trinary **storage** device;
the decrementor unit receiving the data tryte from the second trinary storage device and decrementing each trit of the data tryte one trinary level;
the incrementor unit receiving the data tryte from the **second** trinary **storage** device and incrementing each trit of the data tryte one trinary level;
the **multiplexor** unit receiving: each incremented trit from the incrementor unit, each decremented trit from the decrementor unit, each data tryte from the **second** trinary **storage** device, and each of the output signals from the single **error detector** ;
wherein the **multiplexor** unit under control of the output signals from the single **error detector** selects either the incremented trit, or the decremented trit, or the data trit for each trit position of the tryte for gating the selected trits...

8/3,K/27 (Item 27 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00341188
Storage subsystem including an error correcting cache.
Speichersubsystem mit Fehlerkorrekturcache-Speicher.
Sous-systeme de memoire a antememoire de correction d'erreur.
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
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Gregor, Steven Lee, 628 Church Street, Endicott New York 13760, (US)
Li, Hehching Harry, 39 Cooventry Road, Endicott New York 13760, (US)
LEGAL REPRESENTATIVE:
Schafer, Wolfgang, Dipl.-Ing. (62021), IBM Deutschland Informationssysteme GmbH Patentwesen und Urheberrecht, D-70548 Stuttgart, (DE)
PATENT (CC, No, Kind, Date): EP 348616 A2 900103 (Basic)
EP 348616 A3 910313
EP 348616 B1 951011
APPLICATION (CC, No, Date): EP 89106935 890418;

PRIORITY (CC, No, Date): US 212432 880628
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-012/08; G06F-011/10;
ABSTRACT WORD COUNT: 108

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	638
CLAIMS B	(English)	EPAB95	558
CLAIMS B	(German)	EPAB95	516
CLAIMS B	(French)	EPAB95	654
SPEC A	(English)	EPABF1	77953
SPEC B	(English)	EPAB95	77946
Total word count - document A			78600
Total word count - document B			79674
Total word count - documents A + B			158274

...SPECIFICATION command and address to processor storage and selecting the memory cards in the desired port. Data are transferred 16 bytes at a time across a **multiplexed** command/address and data interface with the L3 memory port. Eight transfers from L3 **memory** are required to obtain the 128-byte L2 cache line. The sequence of quadword transfers starts with the quadword containing the double-word requested by...
...appropriate processor inpage complete to L2 control. During the data transfers to L2 cache, address/key monitors the L3 uncorrectable error lines. Should an uncorrectable **error** be **detected** during the inpage process several functions are performed. With each double-word transfer to the L1 cache, an L3 uncorrectable error signal is transferred simultaneously...

...storage uncorrectable error indication for a given inpage request, the first one detected by address/key. The double-word address of the first storage uncorrectable **error** **detected** by address/key is recorded for the requesting

8/3,K/28 (Item 28 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00312324
Self-testing memory arrangement and method.
Selbstprufendes Speichersystem und Methode.
Dispositif et methode de memoire auto-testante.
PATENT ASSIGNEE:
DIGITAL EQUIPMENT CORPORATION, (313080), 146 Main Street, Maynard, MA 01754, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Lipcon, Jesse B., 23 Deerfoot Trail, Harvard Massachusetts 01451, (US)
Maskas, Barry A., 40-10 Royal Crest Drive, Marlboro Massachusetts 01752, (US)
Morgan, David K., 45 Teresa Road, Hopkington Massachusetts 01748, (US)
LEGAL REPRESENTATIVE:
Goodman, Christopher et al (31122), Eric Potter & Clarkson St. Mary's Court St. Mary's Gate, Nottingham NG1 1LE, (GB)
PATENT (CC, No, Kind, Date): EP 292206 A1 881123 (Basic)
EP 292206 B1 930929
APPLICATION (CC, No, Date): EP 88304331 880513;
PRIORITY (CC, No, Date): US 49812 870514
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G11C-029/00;
ABSTRACT WORD COUNT: 56

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	2232

CLAIMS B	(German)	EPBBF1	898
CLAIMS B	(French)	EPBBF1	1215
SPEC B	(English)	EPBBF1	9124
Total word count - document A			0
Total word count - document B			13469
Total word count - documents A + B			13469

...SPECIFICATION of the bank latches 510, 515, 520 or 525, and therefore, the contents of the corresponding memory locations stored in those latches, differ from the **contents of memory** latch 500, which contains the contents at the corresponding location of bank 0 **of** board 1. In the preferred embodiment, counter 560 is only a seven-bit counter. If there are more than 2(**sup** 7) **errors** , then an overflow (OV) bit is set.

In the preferred embodiment of this invention, memory board 70 is implemented as a ten-bit slice, and...

...the highest order ten lines of memory data bus 65, are stored in register 227 and read from that register by CPU 20 in a **separate memory** read instruction.

The output of counter 560 is an input into the test/sig **multiplexer** 175 and can be output onto memory data bus 65 for input into CPU 10 at the end of the testing procedure. Preferably, this occurs during the first read operation after the diagnostic testing operation. Specifically, when CPU 20 finishes a **test** , it changes the **contents** of register 228 which deasserts lines 0, 10, 20, and 30 of memory data bus 65. In response, test control logic 190 deasserts the TEST...

8/3,K/34 (Item 34 from file: 348)

00264212

Method for diagnosing and testing an interface unit.
Verfahren zur Diagnose und Prufung eines Schnittstellenbausteins.
Methode pour diagnostiquer et tester un ensemble d'interface.

PATENT ASSIGNEE:
Siemens Aktiengesellschaft, (200520), Wittelsbacherplatz 2, W-8000 Munchen 2, (DE), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;NL;SE)
INVENTOR:
Steis, Bruno, Dipl.-Ing., Grosshadernerstrasse 25, W-8000 Munchen 70, (DE)
Jugel, Alfred, Priessnitzweg 13, W-8192 Geretsried, (DE)
Martin, Horst, Dipl.-Phys., Simmerlein-Platz 11, W-8000 Munchen 50, (DE)

PATENT (CC, No, Kind, Date): EP 274653 A2 880720 (Basic)
EP 274653 A3 880803
EP 274653 B1 910807
APPLICATION (CC, No, Date): EP 87117979 871204;
PRIORITY (CC, No, Date): DE 3643099 861217
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: H04M-003/24; H04Q-011/04;
TRANSLATED ABSTRACT WORD COUNT: 94
ABSTRACT WORD COUNT: 70

LANGUAGE (Publication,Procedural,Application): German; German; German

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	443
CLAIMS B	(German)	EPBBF1	334
CLAIMS B	(French)	EPBBF1	507
SPEC B	(German)	EPBBF1	1815
Total word count - document A			0
Total word count - document B			3099
Total word count - documents A + B			3099

...CLAIMS B1

1. Method for diagnosing and testing an interface unit for connecting a

PCM transmission link of a digital time-division **multiplex** telecommunication system to an exchange in a telecommunication system, which, in addition to **other** components, exhibits a speech **memory** for adapting the timing of the pulse frame formed on the transmission link to the pulse frame on which the operation of the exchange is...

...with a parity bit field related either in each case to a channel-individual memory cell and after a reading-out is subjected to a **parity check** (U-SM), or, under control by a higher-priority control system of the exchange, after a switching-related blocking of the relevant channel, a bit...

...of the interface unit is nondestructively read out and is in each case compared with a nominal information, and in that, for the purpose of **error** locating and for **checking** the interface unit, optional test loops comprising different components of the interface unit are formed under initiation by the higher-priority control system before operation is started in the case of proper operation of the interface unit which was interrupted or had not yet been started, a **parity check** covering the content of two pulse frames being performed in the case of the test loop used for checking the speech memory. ...

8/3,K/35 (Item 35 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00259475

Fault tolerant computer achitecture.

Fehlertolerante Rechnerarchitektur.

Architecture de calculateur tolerant les fautes.

PATENT ASSIGNEE:
BULL HN INFORMATION SYSTEMS ITALIA S.p.A., (284245), Via Martiri d'Italia 3, I-10014 Caluso (Torino), (IT), (applicant designated states: DE;FR;GB)
INVENTOR:
Tiziano, Maccianti, Via Pascoli 5, I-20010 Pregnana Milanese, (IT)
Luciano, Raimondi, Via Marghera 3, I-20149 Milano, (IT)
LEGAL REPRESENTATIVE:
Falcetti, Carlo et al (42244), Jacobacci, Casetta & Perani S.p.A, Via Visconti di Modrone, 7, I-20122 Milano, (IT)

PATENT (CC, No, Kind, Date): EP 260584 A2 880323 (Basic)
EP 260584 A3 900509
EP 260584 B1 930804
APPLICATION (CC, No, Date): EP 87113151 870909;
PRIORITY (CC, No, Date): IT 8621727 860917
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-011/16; G06F-011/26;
ABSTRACT WORD COUNT: 160

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	596
CLAIMS B	(German)	EPBBF1	578
CLAIMS B	(French)	EPBBF1	646
SPEC B	(English)	EPBBF1	7244
Total word count - document A			0
Total word count - document B			9064
Total word count - documents A + B			9064

...SPECIFICATION data"leads of system bus BUS B.

The four "parity bit" leads of BUS B (channel 16) are connected to an input set of a **multiplexer** 25.

A second input set of **multiplexer** 25 receives **the parity** bits in **output** from local **memory** 13.

Multiplexer 25 selectively transfers to output channel CK the signals received at one of the input sets.

Channel PM2B0:31 is connected to 32 inputs of a **parity** bit generator/ **checker** CK GEN **26** .
Other four inputs of CK GEN 16 are connected to channel CK.
When generator 26 works as a parity generator, it provides in output for each...

8/3,K/40 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00827955 **Image available**
PROCESSOR HAVING REPLAY ARCHITECTURE WITH FAST AND SLOW REPLAY PATHS
PROCESSEUR A ARCHITECTURE DE REEXECUTION COMPORTANT DES CHEMINS DE REEXECUTION RAPIDES ET LENTS
Patent Applicant/Assignee:
INTEL CORPORATION, 2200 Mission College Blvd., Santa Clara, CA 95052, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
UPTON Michael D, 1410 NW 24th Avenue, Portland, OR 97210, US, US (Residence), US (Nationality), (Designated only for: US)
SAGER David A, 9540 N.W. Skyview Drive, Portland, OR 97231, US, US (Residence), US (Nationality), (Designated only for: US)
BOGGS Darrell D, 2200 S.W. 195th Avenue, Aloha, OR 97006, US, US (Residence), US (Nationality), (Designated only for: US)
HINTON Glenn J, 6130 N.W. 185th Avenue, Portland, OR 97229, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
MALLIE Michael J (et al) (agent), Blakely, Sokoloff, Taylor & Zafman LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, CA 90025, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200161480 A1 20010823 (WO 0161480)
Application: WO 2000US35590 20001229 (PCT/WO US0035590)
Priority Application: US 2000503853 20000214
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 6151

Fulltext Availability:
Detailed Description

Detailed Description
... to be replayed from the first checker 545, another input instruction to be replayed ftorn the second checker 555, and also a manufactured instruction from **another** unit (e.g., the **memory** control or execution unit). In one embodiment, the **multiplexor** 521 gives a low priority to instructions coming from the instruction cache, a medium priority to replay instructions coming ...a high priority to replay instructions coming from the second checker, and a highest priority to manufactured instructions.

As mentioned above, in one embodiment, the **error** conditions **detected** by the first checker 545 can be a subset of the error conditions detected by the second checker 555. In this case, the second checker...

8/3,K/41 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00752029 **Image available**
PROCESS CONTROL SYSTEM WITH INTEGRATED SAFETY CONTROL SYSTEM
SYSTEME DE COMMANDE DE PROCESSUS, A UNITE DE COMMANDE DE SECURITE INTEGREE
Patent Applicant/Assignee:
THE DOW CHEMICAL COMPANY, 2030 Dow Center, Midland, MI 48674, US, US (Residence), US (Nationality)
Inventor(s):
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QUELLE Ernst W, Schoelischer Hochfeld 43, D-21682 Stade, DE
BEZECNY Helmut A, Zum Horn 7, D-21709 Duedenbuettel, DE
KANSE Johannes C, Tuinstraat 4, NL-4521 BR Biervliet, NL
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LINDESMITH Robert J, 870 South Patterson Road, Midland, MI 48640-8971, US
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GRINWIS Donald, 2201 Burlington, Midland, MI 48642, US
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DUNLAP Dennis J, 32 Draper Way, Attleboro, MA 02703, US
FRANK Brent M, 27 Russet Hill Road, Franklin, MA 02038, US
TIBAZARWA Augustine K, Unit #119, 166 Quincy Shore Drive, Quincy, MA 02171, US
Legal Representative:
SCHULTZ Dale H (agent), Intellectual Property, P.O. Box 1967, Midland, MI 48641-1967, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200065415 A2-A3 20001102 (WO 0065415)
Application: WO 2000US10433 20000418 (PCT/WO US0010433)
Priority Application: US 99130627 19990422; US 2000482386 20000112
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 65721

Fulltext Availability:
Detailed Description

Detailed Description
... Several requirements in the certification process for a safety shutdown system under SIL3 require the detection of stuck buffered outputs, decoder failure, selection of unintended **multiplexing** circuits and **other** like failures that cause the **memory** access errors. CPU 12 can not perform these tasks alone; however, with the benefit of Data And Data Shadow 1 5 Memory 14, CPU 12...

...and affiliated determinism to assure a system appropriately predictable in its operation. Safety certification requires that any Data And Data Shadow Memory 14 memory access **error** is **detected** . Such an **error** is generated due to failure in memory components, buffers, or PLD decoding. If an error occurs, the onboard **error detection** alerts Watchdog 2o 603 to take appropriate action via error line 1072. The **error detection** is to insure that each control computer 1 0 memory read is correct and that wrong data is not sent to the control computer 1...

8/3,K/44 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00190375
SYSTEM FOR MEMORY DATA INTEGRITY
SYSTEME DE CONSERVATION DE L'INTEGRITE DE DONNEES EN MEMOIRE

Patent Applicant/Assignee:
UNISYS CORPORATION,
Inventor(s):
JEPPESEN James Henry III,
WHITTAKER Bruce Ernest,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9107722 A1 19910530
Application: WO 90US6855 19901121 (PCT/WO US9006855)
Priority Application: US 89821 19891122
Designated States: AT BE CH DE DK ES FR GB GR IT JP LU NL SE
Publication Language: English
Fulltext Word Count: 5890

Fulltext Availability:
Claims

Claim
... structure of claim I which includes:
(a) selection means for selecting odd or even parity operation.

3 A memory structure storing data words and having **parity check** functionalit ; comprising:
Y
(a) a first plurality of uniform-sized memory modules connected in lateral parallel configuration wherein each module is connected to a first...

...of claim 4 wherein said auxiliary memory module includes:
(a) an output parity line for each one of said memory modules in said first and **second** plurality of **memory** modules.
The structure of claim 5 wherein said accessing means includes:
(a) **multiplexer** means for selecting which one of said output pariry lines will be connected to provide the parity bit output signal.
- 23
7* The structure of...

...said final output word is composed of twice the number of bits residing in each accessed data word.
The structure of claim 3which includes:
(a) **parity checking** logic means for comparing the final output data word parity with the appropriately related parity bits to sense whether a parity error has occurred.
1 0 A **parity checking** system for **checking** the integrity of data accessed from a ROM/PROM memory structure, comprising:
(a) a memory structure having a plurality of uniformly sized memory chips where...PROM parity chip where each parity bit selected is related to the data word on each one of said common output group data buses;
(d) **parity** logic means for **checking** each one of said k parity bits against the calculated parity of each related data word.
ill The structure of claim 10 where IN" is...